REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Redrawn with changes. Converted drawing to one part-one part number SMD format. Corrected art work for Y and Z packages.	92-11-16	M.A. Frye
C	Redrawn with changes. Added devices 03 and 04. Changes to paragraph 4.2.1. Changes to table I and table IIA. Changed the max lead thickness on case outline Z.	93-09-10	M.A. Frye
D	Added case outlines U and T. Made format changes, editorial changes throughout.	94-01-27	M.A. Frye
E	Changes in accordance with NOR 5962-R198-95.	95-10-05	M.A. Frye
F	Changes in accordance with NOR 5962-R005-97.	96-10-04	Raymond Monnin
G	Updated drawing to current requirements. Editorial changes throughout. - gap	01-11-09	Raymond Monnin

REV	G	G	G																	
SHEET	35	36	37																	
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Mike Frye

DRAWING APPROVAL DATE
91-11-08

REVISION LEVEL
G

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

MICROCIRCUITS, MEMORY, DIGITAL, CMOS 9000 GATE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89823**

SHEET 1 OF 37

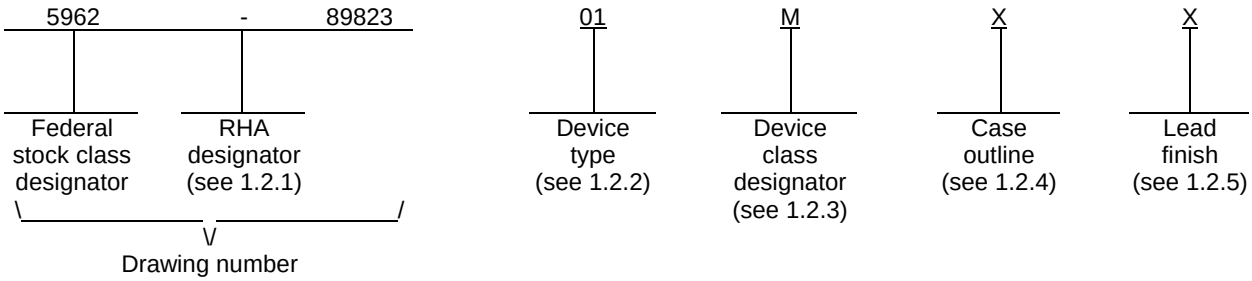
DSCC FORM 2233
APR 97

5962-E003-02

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle Speed
01	3090-50	16 x 20 9000 gate programmable array	50 MHz
02	3090-70	16 x 20 9000 gate programmable array	70 MHz
03	3090-100	16 x 20 9000 gate programmable array	100 MHz
04	3090-125	16 x 20 9000 gate programmable array	125 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA8-PN	175 1/	Pin grid array package
Y	See figure 1	164	Quad flat package
Z	See figure 1	164	Quad flat package
U	See figure 1	164	Quad flat package
T	See figure 1	164	Quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ 175 = actual number of pins used, not maximum listed in MIL-STD-1835

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC} +0.5 V dc
Voltage applied to three-state output(V_{TS})	-0.5 V dc to V_{CC} +0.5 V dc
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	See MIL-STD-1835
Case outlines Y, Z, U, T	20°C/W 3/
Junction temperature (T_J)	+150°C 4/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Case operating temperature Range(T_C)	-55°C to +125°C
Supply voltage relative to ground(V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

_____

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ All voltage values in this drawing are with respect to V_{SS}.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD 78 - IC Latch-Up Test.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Operational notes. Additional information shall be provided by the device manufacturer (see 6.6 herein).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^oC \le T_C \le +125^oC$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8V I_{OH} = -4.0 mA, V_{IH} = 2.0 V	1, 2, 3	All	3.7		V
		V_{CC} = 4.5 V and 5.5 V V_{IL} = 0.9 V and 1.1 V V_{IH} = 3.5 V and 3.85 V I_{OH} = -4.0 mA					
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 4.0V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.4	V
		V_{CC} = 4.5 V and 5.5 V V_{IL} = 0.9 V and 1.1 V V_{IH} = 3.5 V and 3.85 V I_{OH} = 4.0 mA					
Operating power supply current	I_{CC}	V_{CC} = 5.5 V 1/	1, 2, 3	01		245	mA
				02		250	
				03		260	
				04		270	
Quiescent power supply current	I_{CCO}	CMOS inputs, V_{CC} = V_{IN} = 5.5 V	1, 2, 3	All		3.0	mA
Quiescent power supply current	I_{CCO}	TTL inputs, V_{CC} = V_{IN} = 5.5 V	1, 2, 3	All		15	mA
Power-down supply current	I_{CCPD}	PWR DWN = 0.0 V, V_{CC} = V_{IN} = 5.5 V	1, 2, 3	All		2.5	mA
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1, 2, 3	All	-20	20	µA
Output leakage current	I_{OL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1, 2, 3	All	-20	20	µA
Horizontal long line, pull-up current	I_{RLL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1, 2, 3	All		2.5	mA
High level input voltage	V_{IHT}	TTL inputs	1, 2, 3	All	2.0		V
Low level input voltage	V_{ILT}	TTL inputs	1, 2, 3	All		0.8	V
High level input voltage	V_{IHC}	CMOS inputs	1, 2, 3	All	0.7 V_{CC}		V
Low level input voltage	V_{ILC}	CMOS inputs	1, 2, 3	All		0.2 V_{CC}	V
Power down ($\overline{PWR}$ $\overline{DWN}$) voltage 2/	V_{PD}	PWR DWN = 0.0 V	1, 2, 3	All	3.5		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^oC \le T_C \le +125^oC$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance except XTL1 AND XTL2	C_{IN}	See 4.4.1e	4	All		16	pF
Input capacitance XTL1 and XTL2	C_{IN}	See 4.4.1e	4	All		20	pF
Output capacitance	C_{OUT}	See 4.4.1e	4	All		16	pF
Functional test		See 4.4.1c	7, 8A, 8B	All			
Interconnect + t_{PID} + $20(t_{ILO})$ + t_{OP}	t_{B1}	Measured on 20 columns	9, 10, 11	01		304	ns
				02		195	
				03		150	
				04		118	
t_{CKO} + t_{ICK} + t_{CKI} + interconnect	t_{B2}	Tested on all CLB's	9, 10, 11	01		32	ns
				02		21	
				03		18	
				04		15	
t_{CKO} + t_{QLO} + t_{ILO} + t_{DICK} + interconnect	t_{B3}	Tested on all CLB's	9, 10, 11	01		53	ns
				02		34	
				03		26	
				04		22	
t_{ILO} + t_{ECCK} + interconnect	t_{B4}	Tested on all CLB's	9, 10, 11	01		35	ns
				02		23	
				03		19	
				04		17	
t_{OKPO} + t_{OPS} - t_{OPF} + t_{PICK}	t_{B5}	Tested on all CLB's	9, 10, 11	01		73	ns
				02		53	
				03		44	
				04		40	
Interconnect + t_{CKO} + t_{QLO} + t_{PUS} + t_{ICK}	t_{B6}	One long line pull-up	9, 10, 11	01		73	ns
				02		48	
				03		44	
				04		37	
Interconnect + t_{CKO} + t_{QLO} + t_{PUS} + t_{ICK}	t_{B7}	Other long line pull-up	9, 10, 11	01		83	ns
				02		55	
				03		49	
				04		40	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^oC \le T_C \le +125^oC$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + $t_{CKO} + t_{QLO} +$ $t_{IO} + t_{ICK}$	t_{B8}	No pull-up, lower long lines	9, 10, 11	01		47	ns
				02		31	
				03		25	
				04		22	
Interconnect + $t_{CKO} + t_{QLO} +$ $t_{ICK} + t_{IO}$	t_{B9}	No pull-up, upper long lines	9, 10, 11	01		57	ns
				02		38	
				03		32	
				04		28	
Logic input to output (combinational)	t_{ILO}	See figures 4 and 5 as applicable	3/	01		14	ns
				02		9.0	
				03		7.0	
				04		5.5	
Reset input to output	t_{RIO}		3/	01		15	ns
				02		8.0	
				03		7.0	
				04		6.0	
Reset direct width	t_{RPW}		3/	01	12		ns
				02	8.0		
				03	7.0		
				04	6.0		
Master reset pin to CLB output (X, Y)	t_{MRQ}		3/	01		40	ns
				02		34	
				03		31	
				04		30	
K clock input to CLB output	t_{CKO}		3/	01		12	ns
				02		8.0	
				03		6.0	
				04		5.0	
Clock K to the outputs X or Y when Q is return through function generators to drive X or Y	t_{QLO}		3/	01		25	ns
				02		13	
				03		10	
				04		8.0	
K clock logic-input setup	t_{ICK}		3/	01	12		ns
				02	8.0		
				03	7.0		
				04	5.5		

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
K clock logic-input hold	t_{CKI}	See figures 4 and 5 as applicable	3/	All	1.0		ns
Logic input setup to K clock	t_{DICK}		3/	01	8.0		ns
				02	5.0		
				03	4.0		
				04	3.0		
Logic input hold from K clock	t_{CKDI}		3/	01	6.0		ns
				02	4.0		
				03	2.0		
				04	1.5		
Logic input setup to enable clock	t_{ECCK}		3/	01	10		ns
				02	7.0		
				03	5.0		
				04	4.5		
Logic input hold to enable clock	t_{CKEC}		3/	All	2.5		ns
Clock (high) 4/ 5/	t_{CH}		3/	01	9.0		ns
				02	5.0		
				03	4.0		
				04	3.0		
Clock (low) 4/ 5/	t_{CL}		3/	01	9.0		ns
				02	5.0		
				03	4.0		
				04	3.0		
Pad (package pin) to input direct	t_{PID}		3/	01		10.0	ns
				02		6.0	
				03		4.0	
				04		3.0	
Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input	t_{PGCC}		3/	01		8.5	ns
				02		6.5	
				03, 04		6.0	
I/O clock to I/O RI input (FF)	t_{IKRI}		3/	01		11	ns
				02		5.5	
				03		4.0	
				04		3.0	
I/O clock to pad-input setup	t_{PICK}		3/	01	30		ns
				02	20		
				03	17		
				04	16		

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^oC \le T_C \le +125^oC$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
I/O clock to pad-input hold	t_{IKPI}	See figures 4 and 5 as applicable	3/	All	1.0		ns
I/O clock to pad (fast)	t_{OKPO}		3/	01		18	ns
				02		13	
				03		10	
				04		9.0	
I/O clock to pad-output setup	t_{OOK}		3/	01	15		ns
				02	10		
				03	9.0		
				04	8.0		
I/O clock to pad-output hold	t_{OKO}		3/	All	0		ns
I/O clock (high) 5/	t_{IOH}		3/	01	9.0		ns
				02	5.0		
				03	4.0		
				04	3.0		
I/O clock (low) 5/	t_{IOL}		3/	01	9.0		ns
				02	5.0		
				03	4.0		
				04	3.0		
Output (enabled fast) to pad	t_{OPF}		3/	01		15	ns
				02		9.0	
				03		6.0	
				04		5.0	
Output (enabled slow) to pad	t_{OPS}		3/	01		40	ns
				02		33	
				03		24	
				04		20	
Three-state to pad begin high impedance (fast)	t_{TSHZ}		3/	01		14	ns
				02		12	
				03		10	
				04		9.0	
Three-state to pad end high impedance (fast)	t_{TSON}		3/	01		20	ns
				02		14	
				03		12	
				04		11	
Master RESET to input RI	t_{RRI}		3/	01		37	ns
				02		33	
				03, 04		27	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

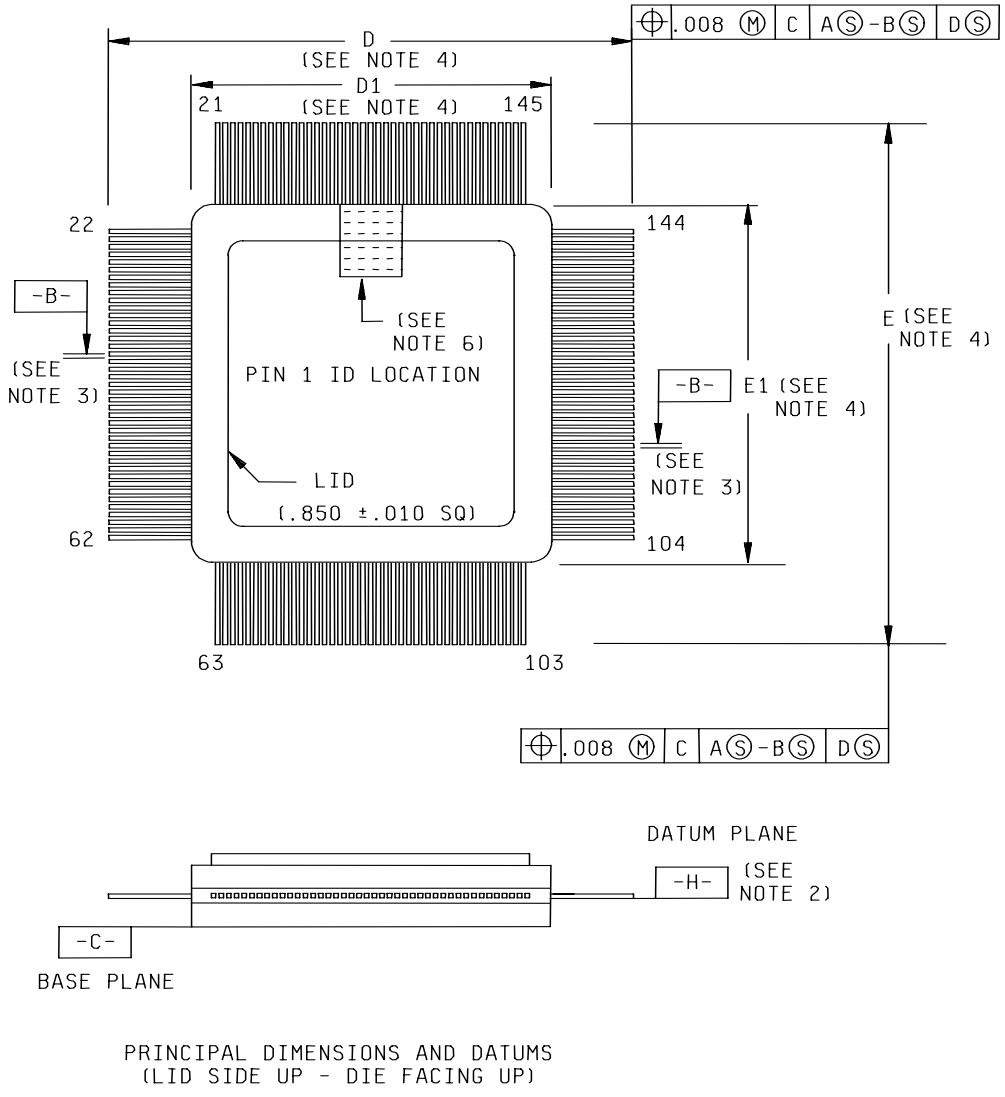
Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Master RESET to output (FF)	t_{RPO}	See figures 4 and 5 as applicable	3/	01		55	ns
				02		47	
				03		34	
				04		32	
Bidirectional buffer delay	t_{BIDI}		3/	01		4.0	ns
				02		2.0	
				03		1.8	
				04		1.7	
TBUF data input to output	t_{IO}		3/	01		8.0	ns
				02		5.0	
				03		4.7	
				04		4.5	
TBUF three-state to output active and valid (single pull-up) double pull-up	t_{ON}		3/	All		17 18	ns
TBUF three-state to output inactive (single pull-up)	t_{PUS}		3/	01		46	ns
				02		38	
				03		26	
				04		26	
TBUF three-state to output inactive (pair of pull-ups)	t_{PUF}		3/	01		22	ns
				02		19	
				03, 04		17	

1/ Tested initially and after any design or process change that may affect this parameter and guaranteed to the limits specified in table I with the following conditions:
Global clock at 16MHz for device 01, and 25 MHz for devices 02, 03, and 04.
20 outputs at 5 MHz
50 outputs at 1 MHz
Alternate clock at 10 MHz
100 configurable logic blocks (CLB) at 5 MHz
150 CLBs at 1 MHz
20 horizontal long lines at 5 MHz
30 vertical long lines at 1 MHz
50 inputs at 5 MHz
10 inputs at 10 MHz

Excessive supply current can occur as a result of internal contention during the initial phase of a reconfiguration following a short interruption of V_{CC}. To avoid this excessive current, monitor the dropping of VCC and immediately initiate a reconfiguration, but hold RESET active. This clears the internal configuration register in less that a millisecond, and avoids all later contentions.

2/ $\overline{\text{PWRDWN}}$ transitions must occur during operational V_{CC} levels.
3/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark patterns (t_{B1-9}) are then used to determine the compliance of this parameter. Characterization data is taken initially and after any design or process change which may affect this parameter.
4/ Minimum CLOCK widths for the auxiliary buffer are 1.25 times the t_{CH} and t_{CL}.
5/ These parameters are for clock pulses internal to the chip. Externally applied clock, increases value by 20 percent.

Case Y



PRINCIPAL DIMENSIONS AND DATUMS
(LID SIDE UP - DIE FACING UP)

FIGURE 1. Case outline.

Case Y

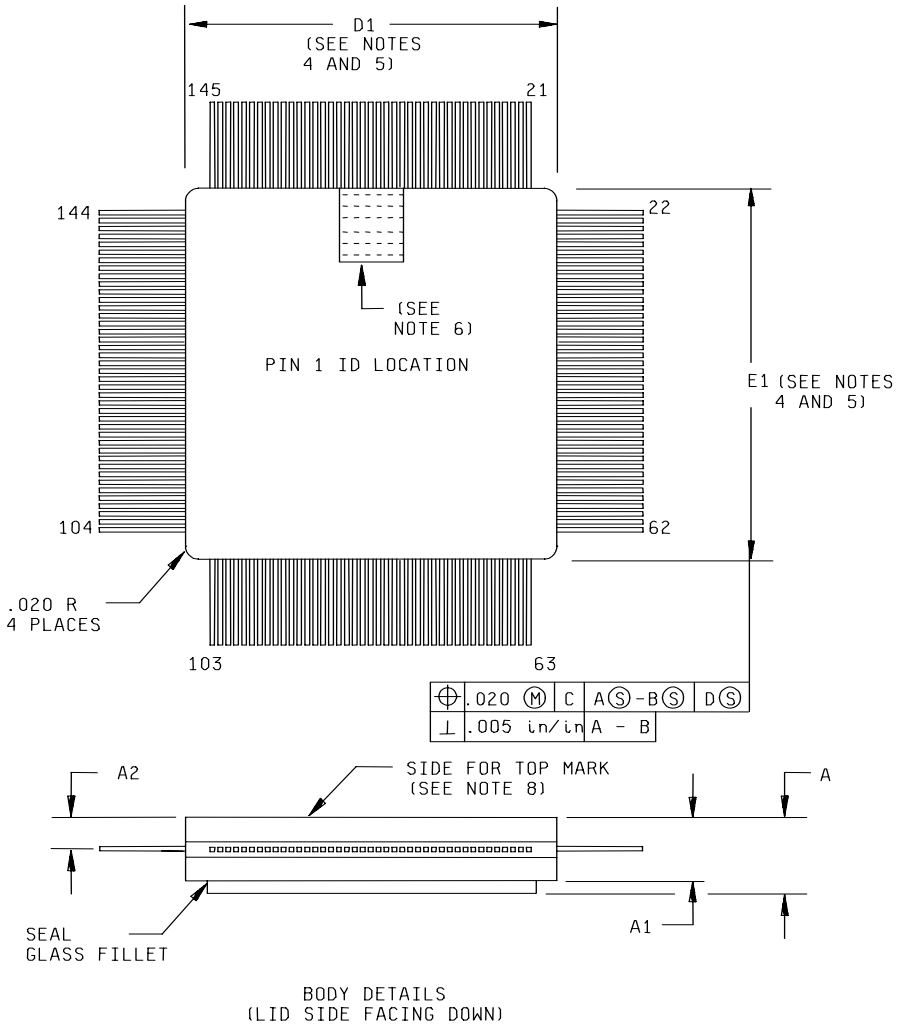


FIGURE 1. Case outline - Continued.

Case Y

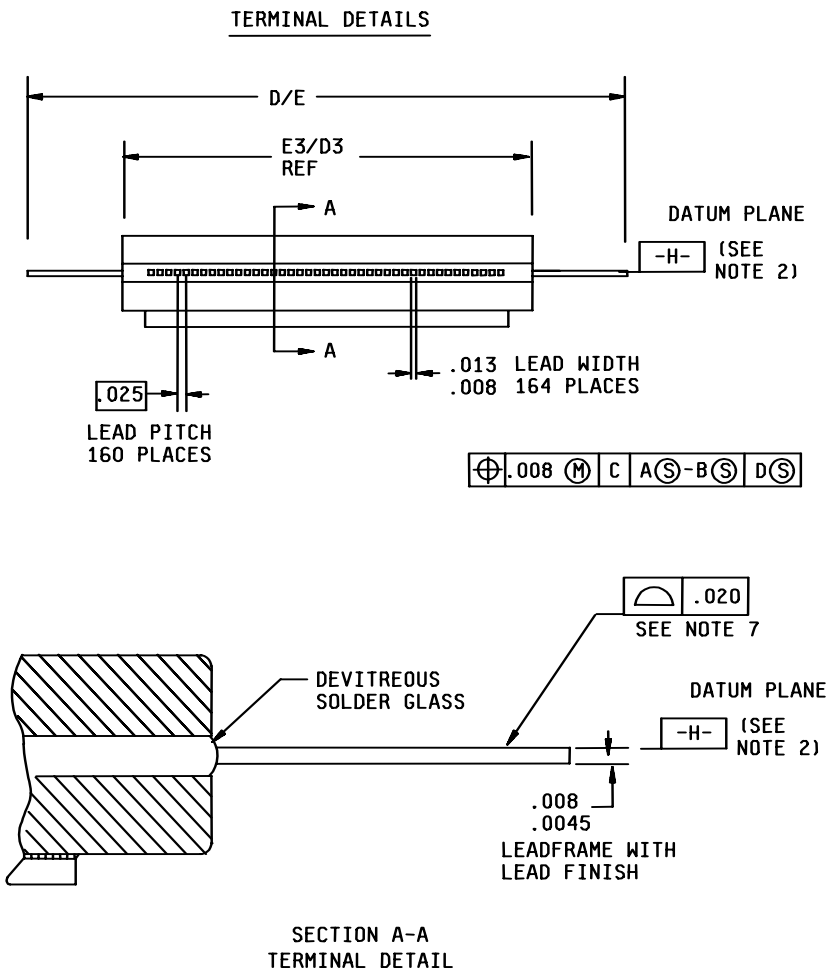


FIGURE 1. Case outline - Continued.

Case Y

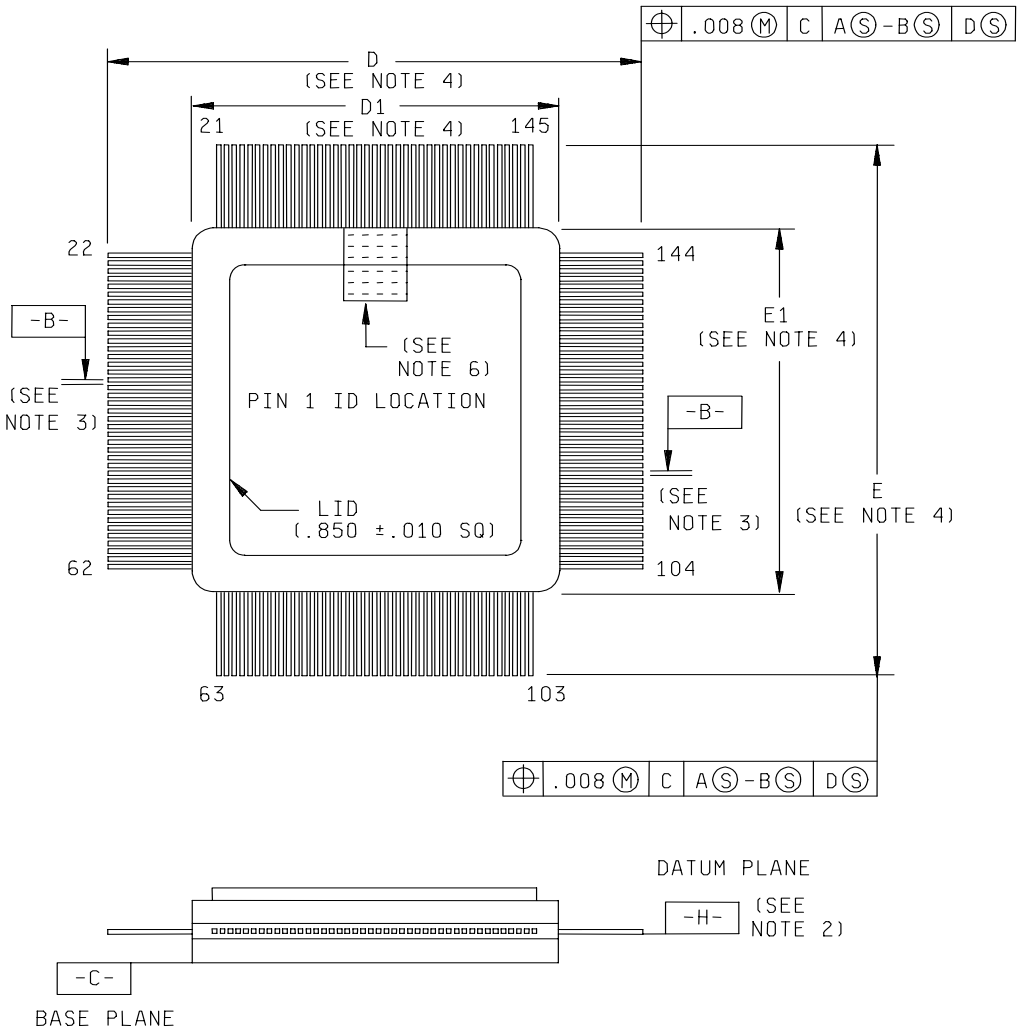
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.125	.145	3.18	3.68	
A1	.100	.120	2.54	3.05	
A2	.060	.070	1.52	1.78	
D	1.510	1.530	38.35	38.86	4
D1	1.060	1.100	26.92	27.94	4, 5
D3	1.000 Ref.		25.40 Ref.		
E	1.510	1.530	38.35	38.86	4
E1	1.060	1.100	26.92	27.94	4, 5
E3	1.000 Ref.		25.40 Ref.		

NOTES

1. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Datum plane -H- is located at the underside of leads, where leads exit package body.
3. Datum A - B and -D- to be determined where center leads exit package body at datum -H-.
4. These dimensions are to be determined at the datum plane -H-.
5. Dimensions D1 and E1 define maximum ceramic body dimensions including glass protrusion and mismatch of ceramic body top and bottom.
6. Pin #1 identifier location. Pin #1 is the middle pin on the side with center justified. Identifier mark may be a notch, dot, or triangle.
7. Packages are shipped with unformed leads
8. Top side mark location, product mark is located on the nonlid side of package; i.e., lid side facing down. When mounted in this position, the pin out is clockwise.

FIGURE 1. Case outline - Continued.

Case U



PRINCIPAL DIMENSIONS AND DATUMS
(LID SIDE UP - DIE FACING UP)

FIGURE 1. Case outline - Continued.

Case U

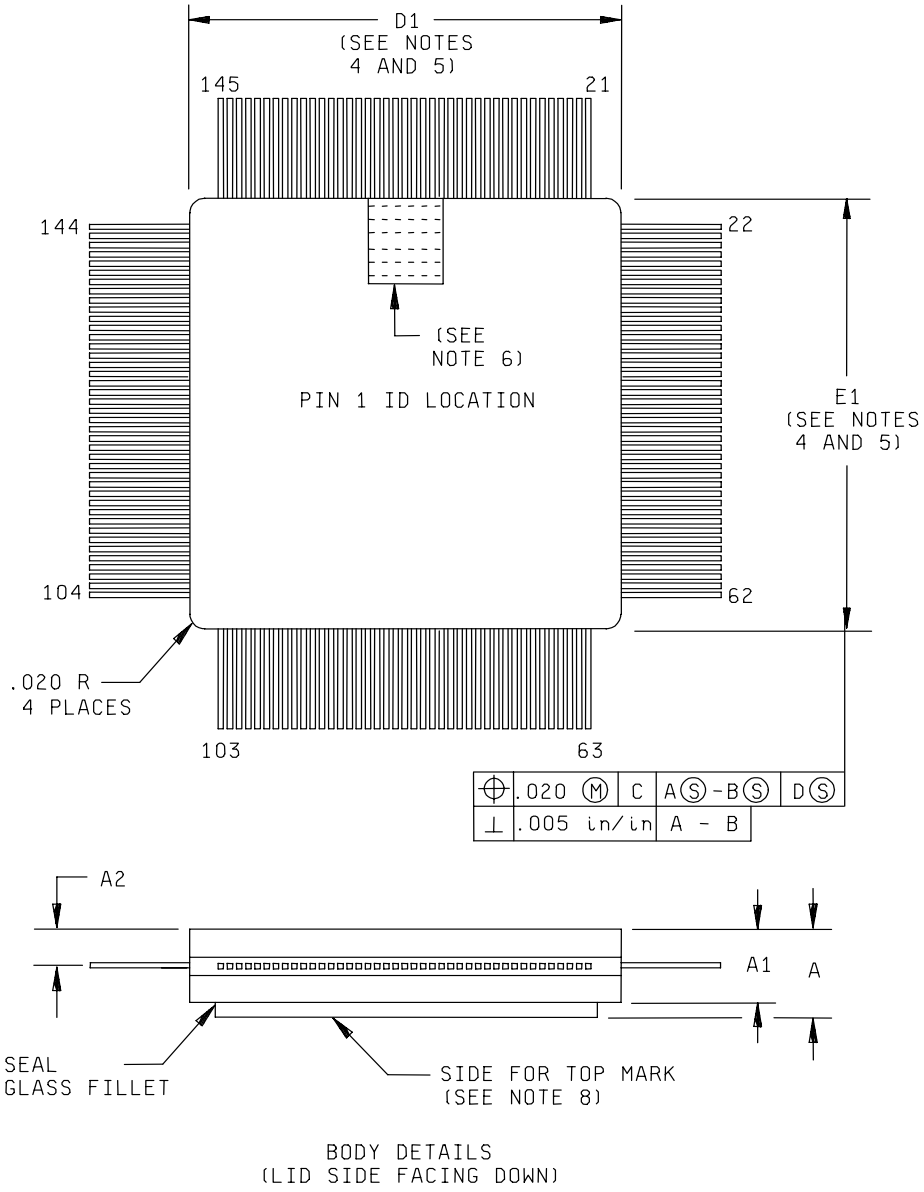


FIGURE 1. Case outline - Continued.

Case U

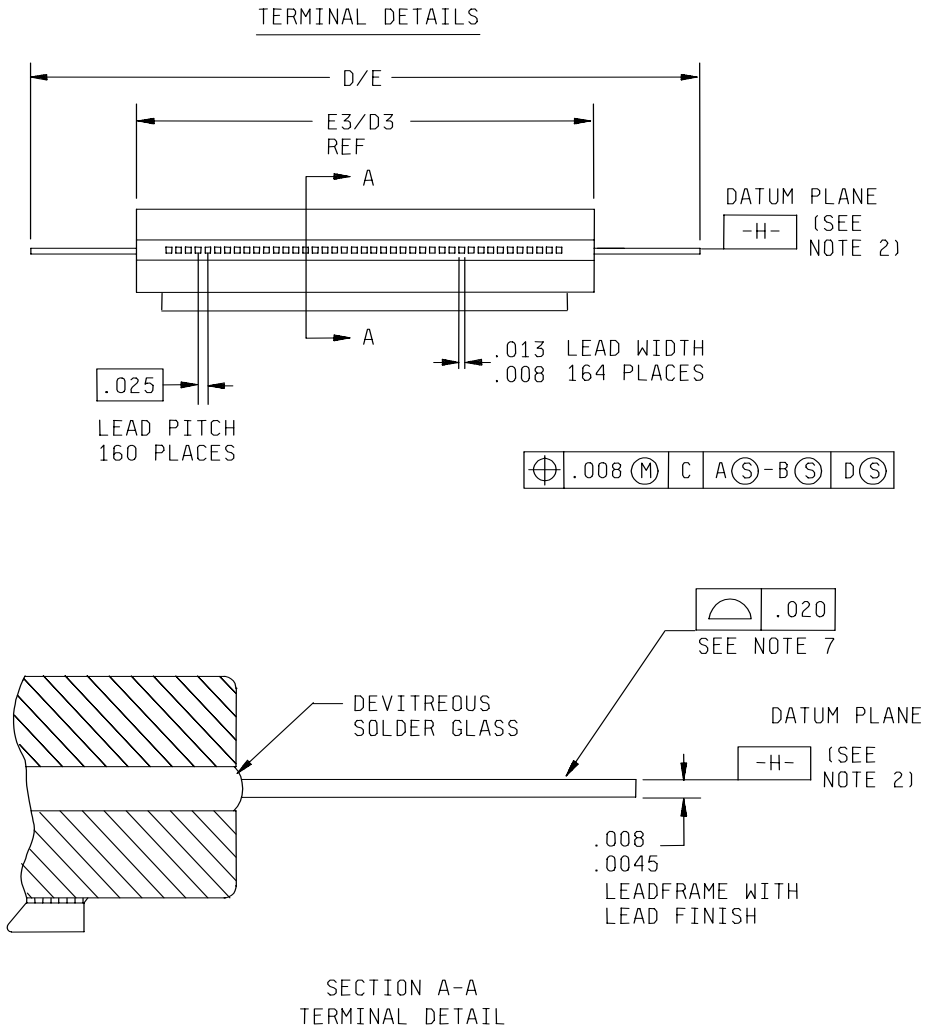


FIGURE 1. Case outline - Continued.

Case U

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.125	.145	3.18	3.68	
A1	.100	.120	2.54	3.05	
A2	.060	.070	1.52	1.78	
D	1.510	1.530	38.35	38.86	4
D1	1.060	1.100	26.92	27.94	4, 5
D3	1.000 Ref.		25.40 Ref.		
E	1.510	1.530	38.35	38.86	4
E1	1.060	1.100	26.92	27.94	4, 5
E3	1.000 Ref.		25.40 Ref.		

NOTES
1. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Datum plane -H- is located at the underside of leads, where leads exit package body.
3. Datum A - B and -D- to be determined where center leads exit package body at datum -H-.
4. These dimensions are to be determined at the datum plane -H-.
5. Dimensions D1 and E1 define maximum ceramic body dimensions including glass protrusion and mismatch of ceramic body top and bottom.
6. Pin #1 identifier location. Pin #1 is the middle pin on the side with center justified. Identifier mark may be a notch, dot, or triangle.
7. Packages are shipped with unformed leads
8. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise.

FIGURE 1. Case outline - Continued.

Cases Z and T (See note 6)

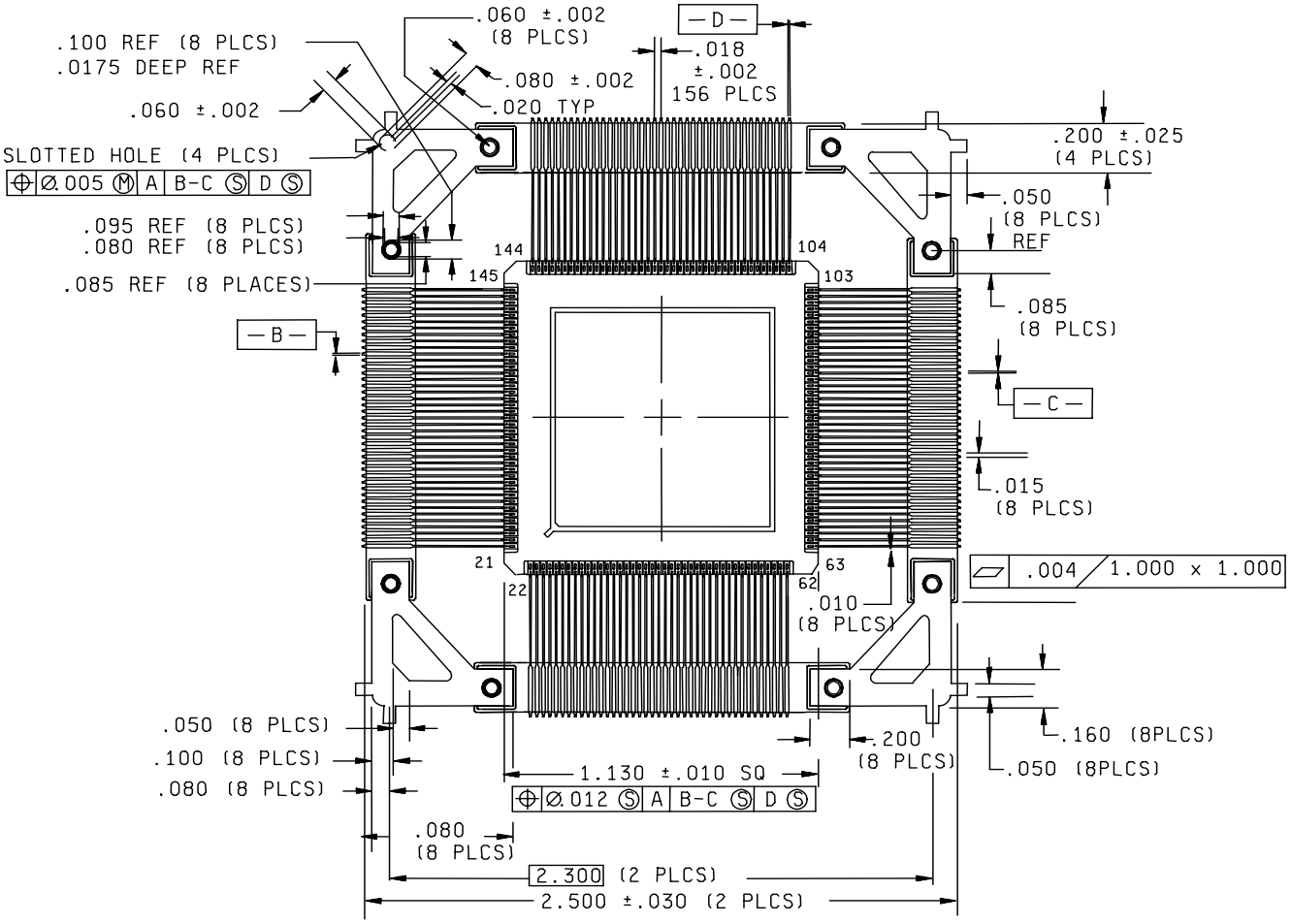
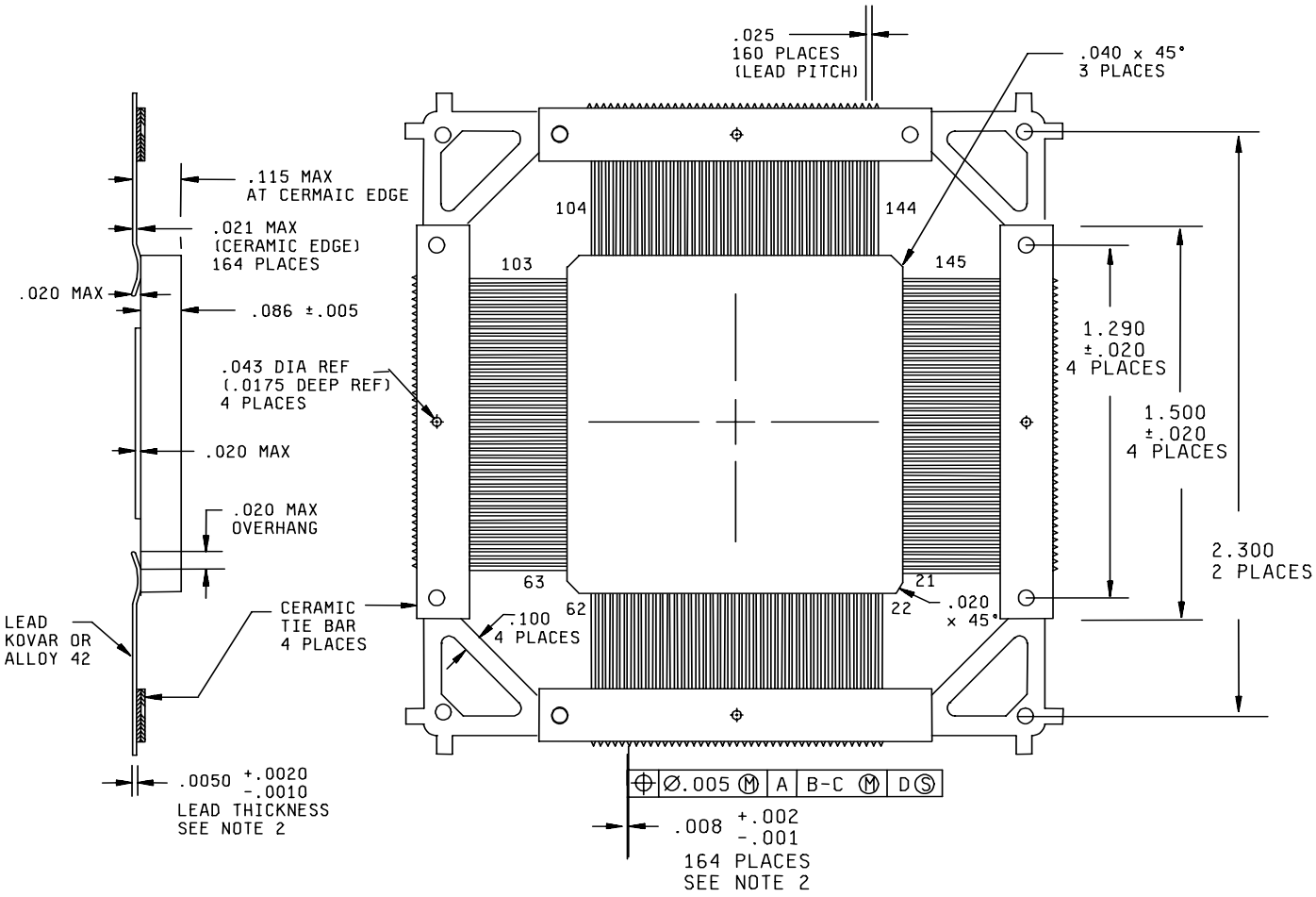


FIGURE 1. Case outline - Continued.

Cases Z and T (See note 6)



NOTES:
1. Dimensions are in inches.
2. Metric dimensions are for reference only.
3. Packages are shipped flat as depicted
4. Lead dimensions call out includes lead finish.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.
6. Case Z represents marking the device on the nonlid side of device, i.e., lid side facing down. When mounted in this position, the pin out is clockwise. Case T represents marking the device on the lid side of the device i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise.

FIGURE 1. Case outline - Continued.

Cases Z and T

Inches	mm	Inches	mm
.0010	0.025	.050	1.27
.001	0.03	.060	1.52
.002	0.05	.080	2.03
.004	0.10	.086	2.18
.005	0.13	.095	2.41
.008	0.20	.100	2.54
.010	0.25	.115	2.92
.012	0.30	.160	4.06
.0175	0.445	.200	5.08
.018	0.46	.645	16.38
.020	0.51	1.000	25.50
.021	0.53	1.130	28.70
.025	0.64	1.290	32.77
.030	0.76	1.500	38.10
.040	1.02	2.300	58.42
		2.500	63.50

NOTE: Metric equivalents are for reference only.

FIGURE 1. Case outline - Continued.

Case outline X

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A2	NC		C1	A8-I/O		D15	$\overline{I/O}$
A3	NC		C2	A9-I/O		D16	LDC-I/O
A4	I/O		C3	GND		E1	A7-I/O
A5	I/O		C4	I/O		E2	I/O
A6	I/O		C5	I/O		E3	A10-I/O
A7	I/O		C6	I/O		E14	HDC-I/O
A8	I/O		C7	I/O		E15	I/O
A9	I/O		C8	I/O		E16	I/O
A10	I/O		C9	I/O		F1	I/O
A11	I/O		C10	I/O		F2	A12-I/O
A12	I/O		C11	I/O		F3	I/O
A13	I/O		C12	I/O		F14	I/O
A14	I/O		C13	I/O		F15	I/O
A15	NC		C14	GND		F16	I/O
A16	NC		C15	M2-I/O		G1	I/O
B1	$\overline{I/O}$		C16	I/O		G2	I/O
B2	PWRDN		D1	A11-I/O		G3	I/O
B3	I/O		D2	I/O		G14	I/O
B4	I/O		D3	V_{CC}		G15	I/O
B5	I/O		D4	TCLKIN-I/O		G16	I/O
B6	I/O		D5	I/O		H1	A6-I/O
B7	I/O		D6	I/O		H2	A13-I/O
B8	I/O		D7	I/O		H3	V_{CC}
B9	I/O		D8	GND		H14	V_{CC}
B10	I/O		D9	V_{CC}			
B11	I/O		D10	I/O		H15	$\overline{INIT}$-I/O
B12	I/O		D11	I/O		H16	I/O
B13	I/O $\overline{\quad}$		D12	I/O		J1	I/O
B14	M1-RDATA		D13	I/O		J2	I/O
B15	M0-RTRIG		D14	V_{CC}		J3	GND
B16	I/O					J14	GND

NC = no connect

FIGURE 2. Terminal connections.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
J15	I/O		N8	GND		R2	CCLK
J16	I/O		N9	V_{CC}		R3	D0-DIN-I/O
K1	A5-I/O		N10	I/O		R4	I/O
K2	A14-I/O		N11	I/O		R5	D1-I/O
K3	I/O		N12	I/O		R6	I/O
K14	I/O		N13	D7-I/O		R7	D2-I/O
K15	I/O		N14	GND		R8	CS1-I/O
K16	I/O		N15	I/O		R9	D4-I/O
L1	I/O		N16	I/O		R10	CS0-I/O
L2	A4-I/O		P1	A2-I/O		R11	I/O
L3	I/O		P2	AO-WS-I/O		R12	I/O
L14	I/O		P3	V_{CC}		R13	I/O
L15	I/O		P4	I/O		R14	DONE-PG
L16	I/O		P5	RDY/BUSY-RCLK-I/O		R15	RESET
M1	A15-I/O		P6	I/O		R16	I/O
M2	I/O		P7	I/O		T1	NC
M3	A1-CS2-I/O		P8	D3-I/O		T2	NC
M14	I/O		P9	I/O		T3	NC
M15	I/O		P10	I/O		T4	I/O
M16	I/O		P11	I/O		T5	I/O
N1	A3-I/O		P12	D6-I/O		T6	I/O
N2	I/O		P13	I/O		T7	I/O
N3	GND		P14	V_{CC}		T8	I/O
N4	DOUT-I/O		P15	XTAL2(IN)-I/O		T9	I/O
N5	I/O		P16	I/O		T10	I/O
N6	I/O		R1	I/O		T11	D5-I/O
N7	I/O					T12	I/O
						T13	I/O
						T14	XTALK1(OUT)-BCLKIN-I/O
						T15	NC
						T16	NC

NC = no connect

FIGURE 2. Terminal connections - Continued.

Case outlines Y, Z, U, and T

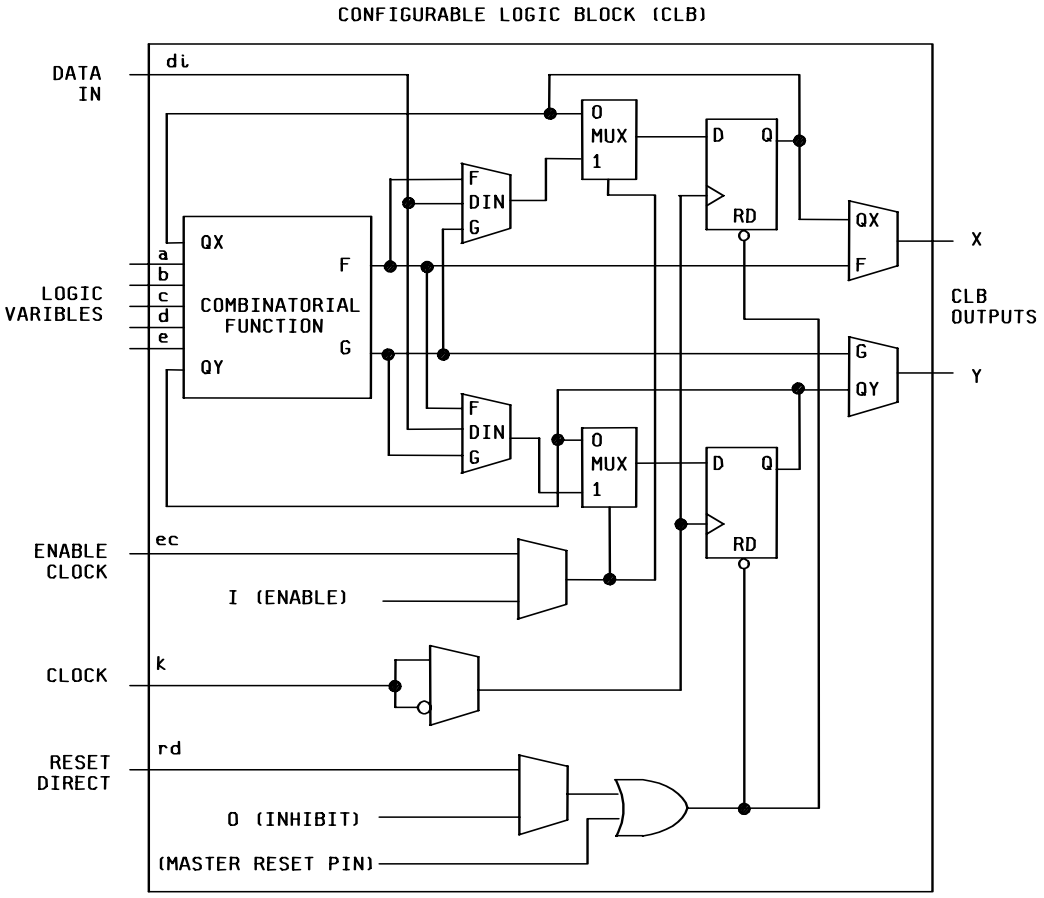
Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	V_{CC}		29	I/O		57	I/O
2	A13-I/O		30	I/O		58	I/O
3	A6-I/O		31	I/O		59	I/O
4	I/O		32	I/O		60	I/O
5	I/O		33	I/O		61	I/O
6	I/O		34	I/O		62	M1-RDATA
7	I/O		35	I/O		63	GND
8	A12-I/O		36	I/O		64	M0-RTRIG
9	A7-I/O		37	I/O		65	V_{CC}
10	I/O		38	I/O		66	M2-I/O
11	I/O		39	I/O		67	HDC-I/O
12	A11-I/O		40	I/O		68	I/O
13	A8-I/O		41	GND		69	I/O
14	I/O		42	V_{CC}		70	I/O
15	I/O		43	I/O		71	LDC-I/O
16	A10-I/O		44	I/O		72	I/O
17	A9-I/O		45	I/O		73	I/O
18	V_{CC}		46	I/O		74	I/O
19	GND		47	I/O		75	I/O
20	PWRDWN		48	I/O		76	I/O
21	TCLKIN-I/O		49	I/O		77	I/O
22	I/O		50	I/O		78	I/O
23	I/O		51	I/O		79	I/O
24	I/O		52	I/O		80	I/O
25	I/O		53	I/O		81	INIT-I/O
26	I/O		54	I/O		82	V_{CC}
27	I/O		55	I/O		83	GND
28	I/O		56	I/O		84	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
85	I/O		112	I/O		139	I/O
86	I/O		113	I/O		140	I/O
87	I/O		114	I/O		141	I/O
88	I/O		115	D5-I/O		142	I/O
89	I/O		116	CSO-I/O		143	D0-DIN-I/O
90	I/O		117	I/O		144	DOUT-I/O
91	I/O		118	I/O		145	CCLK
92	I/O		119	I/O		146	V_{CC}
93	I/O		120	I/O		147	GND
94	I/O		121	D4-I/O		148	A0-WS-I/O
95	I/O		122	I/O		149	A1-CS2-I/O
96	I/O		123	V_{CC}		150	I/O
97	I/O		124	GND		151	I/O
98	I/O		125	D3-I/O		152	A2-I/O
99	XTAL2(IN)-I/O		126	CS1-I/O		153	A3-I/O
100	GND		127	I/O		154	I/O
101	RESET		128	I/O		155	I/O
102	V_{CC}		129	I/O		156	A15-I/O
103	DONE-PG		130	I/O		157	A4-I/O
104	D7-I/O		131	D2-I/O		158	I/O
105	XTAL1(OUT)-BCLKIN-I/O		132	I/O		159	I/O
			133	I/O		160	A14-I/O
106	I/O		134	I/O		161	A5-I/O
107	I/O		135	I/O		162	I/O
108	I/O		136	I/O		163	I/O
109	D6-I/O		137	D1-I/O		164	GND
110	I/O		138	RDY/BUSY-RCLK-I/O			
111	I/O						

FIGURE 2. Terminal connections - Continued.

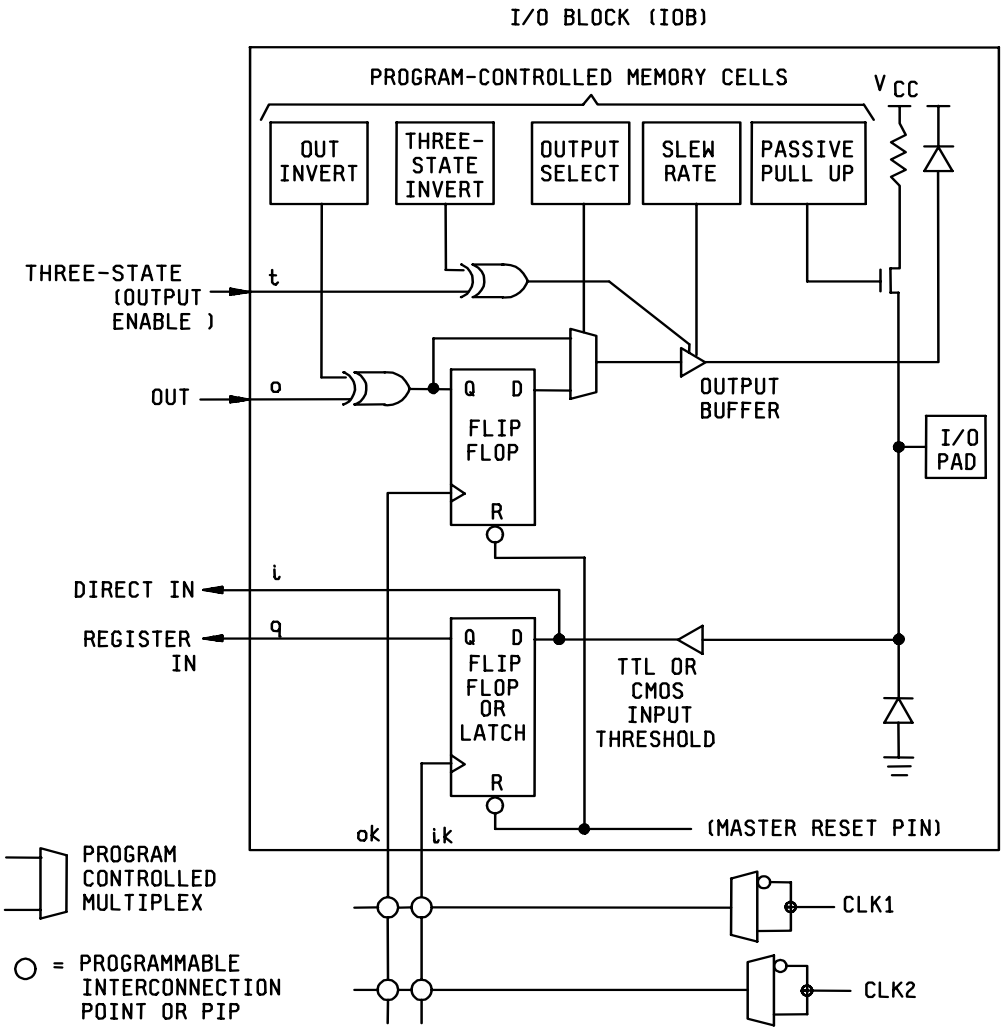
CONFIGURABLE LOGIC BLOCK (CLB)



NOTE: Each configurable logic block includes a combinatorial logic section, two flip-flops, and program memory controlled multiplexer selection of function.

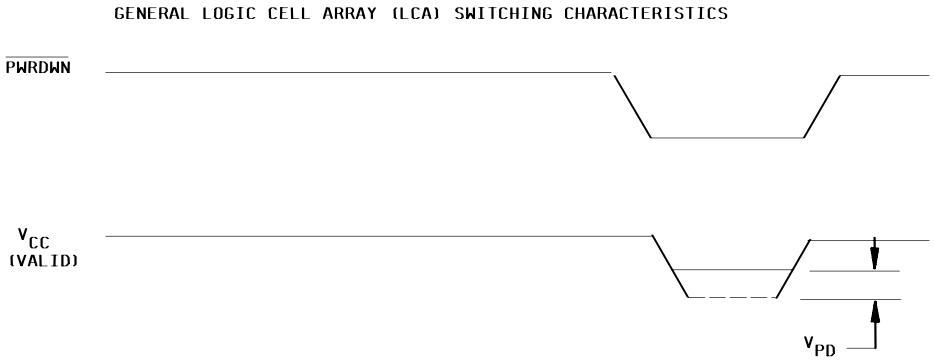
It has: Five logic variable inputs: a, b, c, d, and e.
a direct data input: di
an enable clock: ec
a clock (invertible): k
an asynchronous reset: rd
two outputs: x and y

FIGURE 3. Logic block diagram.



NOTE: The input/output block includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active low latch enable (latch transparent) signal and vice versa. Passive pull-up can only be enable on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

FIGURE 3. Logic block diagram - Continued.



NOTE: All timings except t_{TSHZ} and t_{TSON} are measured at 1.5 V levels with 50 pF minimum output load. For input signals, rise and fall times are less than 6.0 ns, with low amplitude = 0.0 V, and high amplitude = 3.0 V.

FIGURE 4. Timing diagrams and switching characteristics.

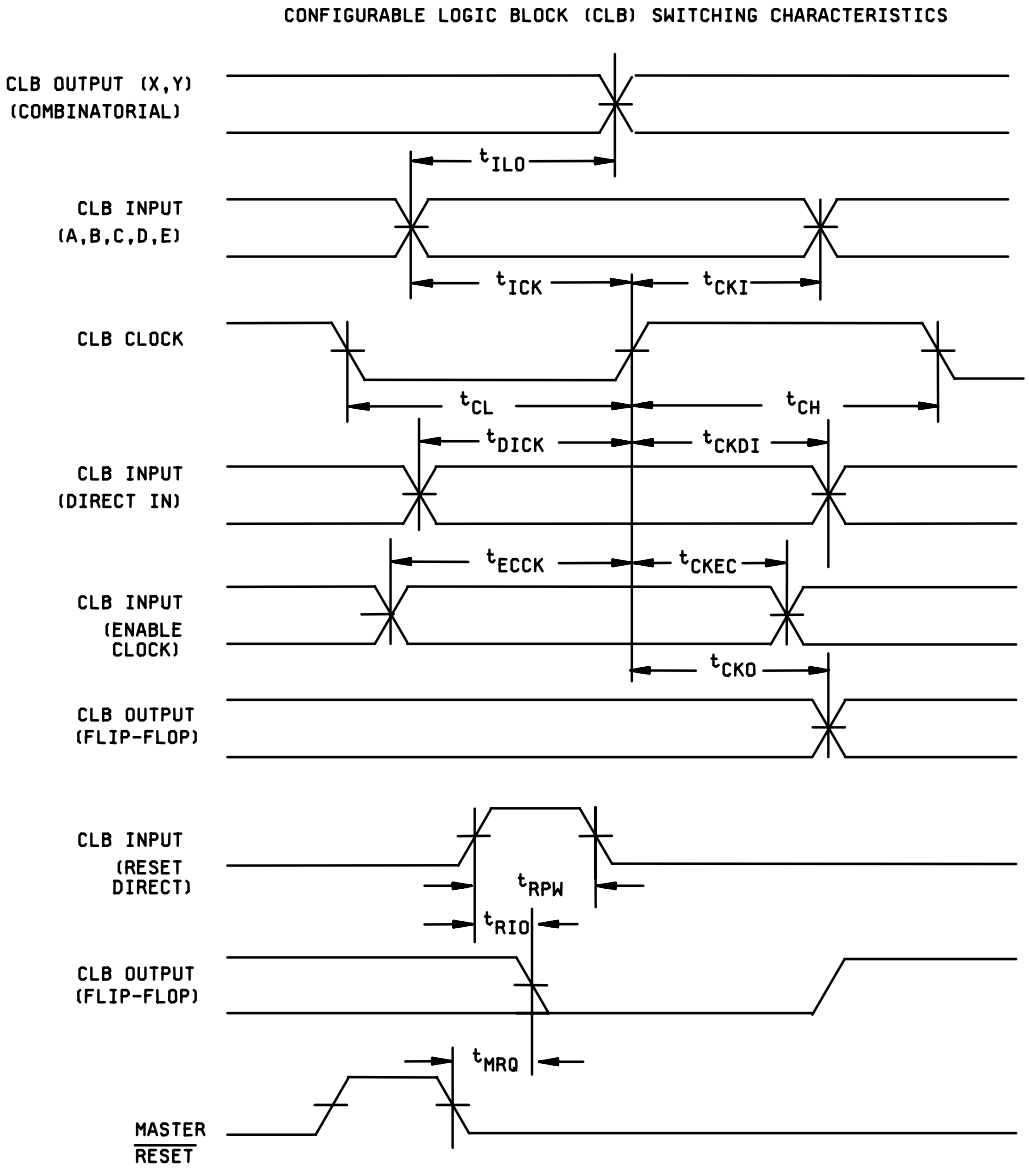
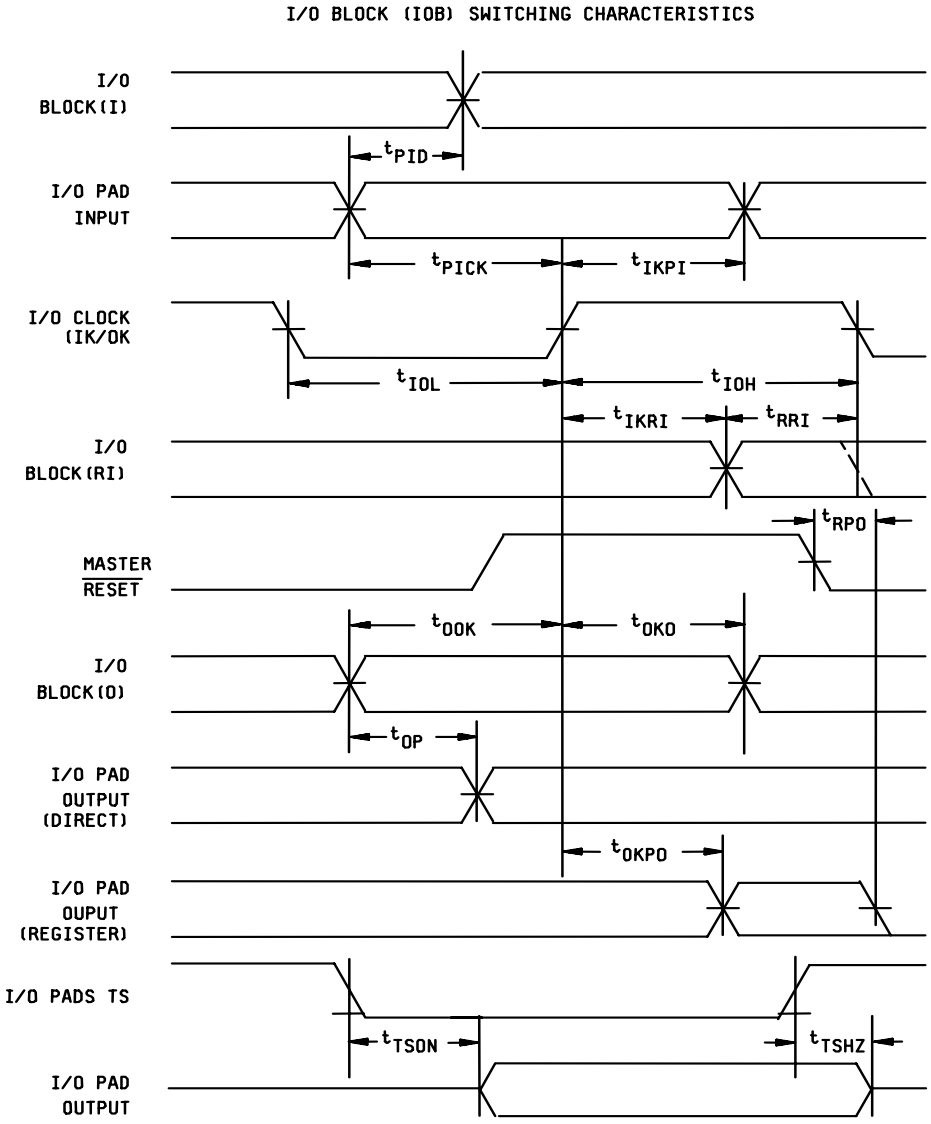
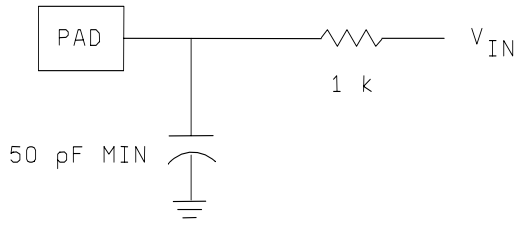


FIGURE 4. Timing diagrams and switching characteristics - Continued.

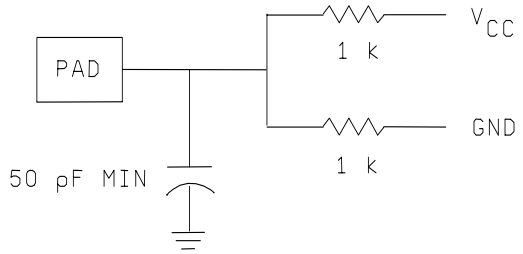


NOTE: All timings except t_{TSHZ} and t_{TSON} are measured at 1.5 V with 50 pF minimum load output. For input signals, rise and fall times are ≤ 6ns, low amplitude = 0 V and high = 3 V. t_{TSHZ} is determined when the output shifts 10 percent (of the output voltage swing) from V_{OL} level or V_{OH} level. See figure 5, circuit A herein for circuit used. t_{TSON} is measured at 0.5 V_{CC} level with V_{IN} = 0.0 for three-state to active high, and $V_{IN} = V_{CC}$ for three-state to active low. See figure 5, circuit B herein for circuit used.

FIGURE 4. Timing diagrams and switching characteristics - Continued.



Circuit A



Circuit B

FIGURE 5. Load circuit.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Not required	Not required	Not required
5	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10 11
6	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CCO} standby	± 300 μA
I_{IL}, I_{OL}	± 2 nA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Symbols, definitions, and functional descriptions.

PWRDWN	POWER-DOWN
M0	MODE 0
RTRIG	READ TRIGGER
M1	MODE 1
RDATA	READ DATA
M2	MODE 2
HDC	HIGH DURING CONFIGURATION
LDC	LOW DURING CONFIGURATION
RESET	RESET
DONE	DONE
PG	PROGRAM
BCLKIN	BCLKIN
XTL1	EXTERNAL CRYSTAL
XTL2	EXTERNAL CRYSTAL
CCLK	CONFIGURATION CLOCK
DOUT	DATA OUT
DIN	DATA IN
CSO	CHIP SELECT, WRITE
CS1	CHIP SELECT, WRITE
CS2	CHIP SELECT, WRITE
WS	CHIP SELECT, WRITE
RCLK	READ CLOCK
RDY/BUSY	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.
TCLKIN	TCLKIN
INIT	INIT
D0-D7	DATA
A0-A15	ADDRESS
I/O	INPUT/OUTPUT(DEDICATED)
V_{CC}	+5.0 V SUPPLY VOLTAGE
GND	GROUND

6.6 Additional operating data.

a. Power on delay is 2^{14} cycles from the non-master mode. This provides 11 to 33 ms of wait time.

b. Power on delay is 2^{16} cycles for the master mode. This provides 43 to 130 ms of wait time.

c. Clear is 375 cycles ±25 cycles and may take as long as 250 to 750 ms.

d. During normal power up, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 10 ms. If this does not occur, configuration must be delayed by using RESET.

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

10. SCOPE

10.1 Scope. This appendix contains the PIN substitution information necessary to support the addition of the device class designator that occurred in revision B dated 92-11-16. SMD 5962-89823MXX supersedes SMD 5962-89823XX. For new designs, after 92-11-16 the NEW PIN shall be used in lieu of the OLD PIN. For existing designs prior to 92-11-16 the NEW PIN can be used in lieu of the OLD PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

20. APPLICABLE DOCUMENTS This section is not applicable to this appendix.

30. SUBSTITUTION DATA

New PIN	Old PIN
5962-8982301MXX	5962-8982301XX
5962-8982301MYX	5962-8982301YX
5962-8982301MZX	5962-8982301ZX
5962-8982301MUX	not originally available
5962-8982301MTX	not originally available
5962-8982302MXX	5962-8982302XX
5962-8982302MYX	5962-8982302YX
5962-8982302MZX	5962-8982302ZX
5962-8982302MUX	not originally available
5962-8982302MTX	not originally available
5962-8982303MXX	not originally available
5962-8982303MYX	not originally available
5962-8982303MZX	not originally available
5962-8982303MUX	not originally available
5962-8982303MTX	not originally available
5962-8982304MXX	not originally available
5962-8982304MYX	not originally available
5962-8982304MZX	not originally available
5962-8982304MUX	not originally available
5962-8982304MTX	not originally available

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-11-09

Approved sources of supply for SMD 5962-89823 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8982301MXC	3/	XC3090-50PG175B
5962-8982301MYA	3/	XC3090-50CQ164B
5962-8982301MZC	3/	XC3090-50CB164B
5962-8982301MUA	3/	XC3090-50CQ164B
5962-8982301MTC	3/	XC3090-50CB164B
5962-8982301QXA	3/	ATT3090-50R175MQ
5962-8982301QZA	3/	ATT3090-50N164MQ
5962-8982302MXC	3/	XC3090-70PG175B
5962-8982302MYA	3/	XC3090-70CQ164B
5962-8982302MZC	3/	XC3090-70CB164B
5962-8982302MUA	3/	XC3090-70CQ164B
5962-8982302MTC	3/	XC3090-70CB164B
5962-8982302QXA	3/	ATT3090-70R175MQ
5962-8982302QZA	3/	ATT3090-70N164MQ
5962-8982303MXC	68994	XC3090-100PG175B
5962-8982303MYA	3/	XC3090-100CQ164B
5962-8982303MZC	68994	XC3090-100CB164B
5962-8982303MUA	3/	XC3090-100CQ164B
5962-8982303MTC	68994	XC3090-100CB164B
5962-8982303QXA	3/	ATT3090-100R175MQ
5962-8982303QZA	3/	ATT3090-100N164MQ
5962-8982304QXA	3/	ATT3090-125R175MQ
5962-8982304QZA	3/	ATT3090-125N164MQ

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124